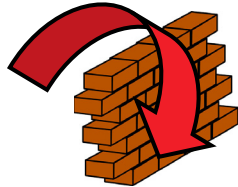


Arx: Bringing RTL to the System Level

Get C++ and VHDL from a Single Source Code

The problem that Arx solves:

- In many companies, system engineers specify DSP algorithms in C or Matlab.
- Then, they throw the specifications “over the wall”, for the RTL engineers to build digital hardware.
- Costly time is lost in recoding C into HDL.



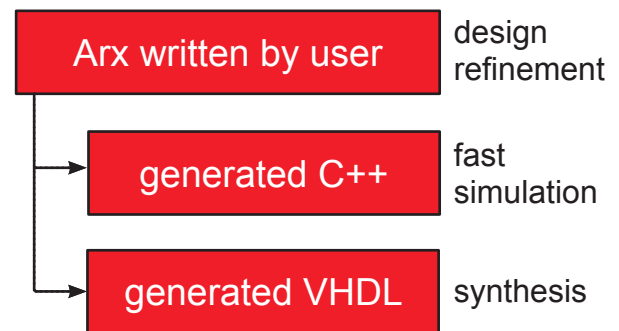
On C-to-HDL translation:

- The argument in favor of C-to-HDL translation is that there is a lot of legacy code in C and there are more software engineers than hardware designers.
- However, the issue is not to learn an HDL but to understand hardware design. A C-programmer does not become a hardware engineer by the mere availability of a C-to-HDL translator!

The Arx approach:

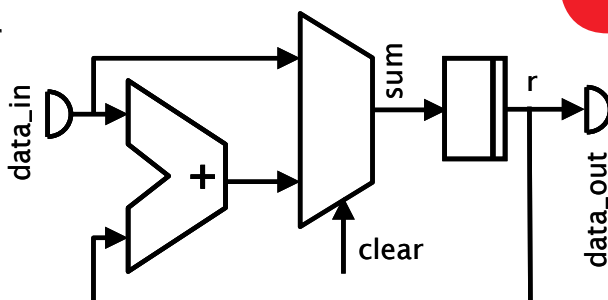
- A domain-specific language expresses the semantics of DSP hardware at the register-transfer level.
- No synthesizable subset: the entire language is always available.
- Code generators generate C for fast zero-delay simulation and VHDL for synthesis.
- Refinement until cycle-accurate and bit-true models.

The Arx workflow:



Example: an accumulator

```
component top
  wl: generic integer = 10
  T_in : generic type = signed(wl, 1)
  T_out: generic type = signed(wl-2, 1, sat, round)
  T_sum: generic type = signed(wl+5, 6)
  clear: in bit
  data_in : in T_in
  data_out: out T_out
variable
  sum: T_sum
register
  r: T_sum = 0
begin
  if clear == 1
    sum = data_in
  else
    sum = r + data_in
  end
  r = sum
  data_out = r
end
```



Arx features:

- Designed with simplicity in mind.
- Explicit distinction between wires and registers.
- Implicit clock and reset.
- Generic data types that can be propagated through the hierarchy.
- Fixed-point data types with various overflow and quantization modes.

Try Arx for free on
www.bibix.nl

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